A Novel Yield Optimization Technique for Digital CMOS Circuits Design by Means of Process Parameters Run-Time Estimation and Body Bias Active Control

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Abstract—This work presents a novel approach to optimize digital integrated circuits yield referring to speed, dynamic power and leakage power constraints. The method is based on process parameter estimation circuits and active control of body bias performed by an on-chip digital controller. The associated design flow allows us to quantitatively predict the impact of the method on the expected yield in a specific design. We present the architecture scheme, the theoretical foundation, the estimation circuits used, and two application case studies, referring to an industrial 0.13-μm CMOS process data. The approach results to be remarkably effective at high operating temperature. In the presented case study, initial yields below 14% are improved to 86% by using a single controller and a single set of estimation circuits per die.

Index Terms—Active body bias, digital CMOS circuits design, process parameters estimation, yield.

I. INTRODUCTION

TRADITIONALLY, the goal of digital circuit designers has been to obtain the best tradeoff between speed (in terms of achievable clock frequency) and power consumption. Recently, the requirement of low power dissipation has become an overarching constraint for microprocessors design in mobile environments. Moreover, as technologies continue to scale following the international technology roadmap for semiconductors (ITRS), power density has become even more significant concern due to its impact on packaging costs. At circuit level, the most important components of power dissipation are dynamic power—due to CMOS switching activity—and leakage power—due to parasitic currents in switched-off CMOS devices—and it is expected that leakage power will become comparable to dynamic power consumption in the very near future [1].

Process parameter variations at the different production levels (i.e., die, wafer, lot, and run) can have a strong impact on circuit performance—in terms of speed, dynamic power and leakage power—possibly compromising the production of most innovative digital integrated circuits (ICs) design due to a too low yield. To achieve an acceptable yield, the designer often refers to process corner values for assessing expected performance figures. Since actual performance figures of merit can thus vary by more than 100% in the extreme cases, it can be necessary to design the circuit with much better performance figures than required in the nominal case, to guarantee that all fabricated circuits meet the expected requirements. A better trade-off between performance and yield can be obtained if a design approach based on statistical tools—such as Monte Carlo analysis—is used, instead of a corner analysis based one.

The yield optimization problem has been addressed and analytically formulated from a statistical point of view in [2], and various approaches, such as design centering [2] or design of experiment (DOE) [3], have been proposed to find computer-aided design (CAD)-oriented solutions. The essential process parameters affecting a CMOS circuit performance are the threshold voltage $V_T$, the conductance parameter $K$, and the transition frequency $f_T$. Both performance and yield of a digital IC would dramatically benefit from having the circuit optimized for the actual CMOS process parameters.

Previous research works have targeted the control of body bias voltage to maximize specific system level macro parameters, such as the sustainable clock frequency, or minimize the leakage power. In [4], the effectiveness of using reverse body bias to reduce leakage power during active operation, burn-in and stand-by has been discussed. In [5], the authors analyze the effects of using adaptive body bias to reduce the impact of die-to-die threshold voltage $V_T$ variations on within-die $V_T$ variations. In [6], forward body bias is used for a communication router design in 150-nm CMOS to obtain 1-GHz operation at 1.1-V supply. In [7], the authors propose the simultaneous use of adaptive body bias and dynamic voltage scaling to reduce power consumption in high performance processors. Analytical models of the leakage current, dynamic power and frequency as functions of body bias are also derived. In [8], adaptive body bias is used to compensate for die-to-die parameter variations by applying the body bias that maximizes the die frequency subject to a power constraint.

Finally, in [9], adaptive $V_{DD}$ and body bias are jointly used to reduce the impact of parameter variations on frequency, dynamic power, and leakage power of microprocessors. In many cases, it is assumed that within-die parameter variations are much lower than die-to-die parameter variations [10], and the effects of within-die fluctuations are neglected by following a worst-case approach [10], [11]. However, as pointed out in [12], the effects of within-die fluctuations increase as the channel